CLAIMS

What is claimed is:

1. A circuit arrangement for generating non-overlapping clock phases, comprising:

a first circuit unit combining two input signals to form an output signal, a first input of the first circuit unit provided for application of a common clock signal;

a second circuit unit combining two input signals to form an output signal, a first input of the second circuit unit provided for application of the common clock signal; and

a first multiplexer unit having a first input connected to an output of the first circuit unit, a second input connected to an output of the second circuit unit, and an output connected to a second input of each of the first and second circuit units, and having a third input that switches between the first and second inputs of the first multiplexer unit for application of the clock signal,

wherein a plurality of non-overlapping clock phases are provided by output signals of the first and second units and of the first multiplexer unit.

2. The circuit arrangement as claimed in claim 1, further comprising a second multiplexer unit connected between the first circuit unit and the first multiplexer unit, wherein a first input of the second multiplexer unit is connected to the output of the first circuit unit, a second input of the second multiplexer unit is connected to the output of the first multiplexer unit, and an output of the second multiplexer unit is connected to the first input of the first multiplexer unit and the second input of the first switching unit, and a third input of the second multiplexer unit is provided for application of the clock signal.

3. The circuit arrangement as claimed in claim 2, further comprising additional multiplexer units connected between the first circuit unit and the multiplexer unit nearest thereto, wherein each of the additional multiplexer units is connected in a manner similar to that of the second multiplexer unit between the first circuit unit and the first multiplexer unit.

4. The circuit arrangement as claimed in claim 1, wherein each of the first and second circuit units includes a NAND element with a delay element coupled downstream from the NAND element, and wherein an inverter is coupled upstream of the first input of the second circuit unit.

5. The circuit arrangement as claimed in claim 1, wherein each of the first and second circuit units includes a NOR element with a delay element coupled downstream from the NOR element, and wherein an inverter is coupled upstream of the first input of the second circuit unit.

6. The circuit arrangement as claimed in one of claim 1, wherein the first multiplexer unit includes a multiplexer and a delay element connected downstream from the multiplexer, and wherein the first and second inputs of the first multiplexer unit are data inputs of the multiplexer and the third input of the multiplexer unit is the switch input of the multiplexer.